IN THE CLAIMS:

Please amend the following claims having the same number as indicated:

1. (Currently Amended). A controller, comprising:

a primary processing unit;

a secondary processing unit coupled to the primary processing unit;

a common memory coupled to the primary and secondary processing units, the common memory containing a control algorithm, wherein the primary and secondary processing units are adapted to run the control algorithm; ~~and,~~

a functional compare module coupled to the primary processing unit and the secondary processing unit for comparing a primary output of the primary processing unit and a secondary output of the secondary processing units after the control algorithm has been run by the primary and secondary processing units; and,

at least one bus, wherein the common memory, primary and secondary processing units, and function compare module are coupled to the at least one bus, wherein the functional compare module is adapted to read signals on the at least one bus, generate a signature of the signals, compare the generated signature with a reference signal and detect a fault is the signals are not the same.

2. (Original). A controller, as set forth in claim 1, wherein the functional compare module is adapted to detect a fault if the primary output and the secondary output are not the same.

3. (Original). A controller, as set forth in claim 1, wherein the primary output and the secondary output are data.

4. (Original). A controller, as set forth in claim 1, wherein the primary output and the secondary output are control signals.

5. (Original). A controller, as set forth in claim 1, wherein the functional compare module is adapted to perform diagnostics upon startup of the controller.

6. (Currently Amended). A controller, ~~as set forth in claim 1, including~~ comprising:

a primary processing unit;

a secondary processing unit coupled to the primary processing unit;

a common memory coupled to the primary and secondary processing units, the common memory containing a control algorithm, wherein the primary and secondary processing units are adapted to run the control algorithm;

a functional compare module coupled to the primary processing unit and the secondary processing unit for comparing a primary output of the primary processing unit and a secondary output of the secondary processing units after the control algorithm has been run by the primary and secondary processing units; and,

at least one peripheral module coupled to the primary processing unit, wherein the at least one peripheral nodule includes a built in self test circuit for detecting faults within the peripheral module, the built in self test circuit being coupled to the primary processing unit.

7. (Cancelled).

8. (Currently Amended). A controller, as set forth in claim 1 ~~7~~, wherein the at least one bus includes an address bus, a data bus, and a control bus.

9. (Original). A controller, as set forth in claim 1, wherein the primary processing unit is coupled to a system for control of the system, and wherein the secondary processing unit is adapted to control the system if a fault is detected in the primary processing unit.

10. (Original). A controller, as set forth in claim 9, wherein the secondary processing unit is coupled to a second system for control of the second system.

11. (Currently Amended). A method for detecting a fault in a controller, the controller including a primary processing unit, a secondary processing unit coupled to the primary processing unit, ~~and~~ a common memory coupled to the secondary and primary processing units, and at least one peripheral module coupled to the primary processing unit, including the steps of:

reading a control algorithm stored in the common memory by the primary processing unit;

reading the control algorithm stored in the common memory by the secondary processing unit;

comparing a primary output of the primary processing unit and a secondary output of the secondary processing unit and responsively detecting a fault; and,

detecting a fault within the peripheral module using a built in self test circuit coupled to the primary processing unit.

12. (Original). A method, as set forth in claim 11, wherein the primary output and the secondary output are data.

13. (Original). A method, as set forth in claim 11, wherein the primary output and the secondary output are control signals.

14. (Original). A method, as set forth in claim 11, including the step of performing diagnostics upon startup of the controller.

15. (Cancelled).

16.-19. (Cancelled).

20. (Currently Amended). An apparatus for controlling a first system of a motor vehicle, comprising:

a primary processing unit for performing a first set of functions with respect to the first system;

a secondary processing unit coupled to the primary processing unit;

a common memory coupled to the primary and secondary processing units, the common memory containing a control algorithm, wherein the primary and secondary processing units are adapted to run the control algorithm; ~~and,~~

a functional compare module coupled to the primary processing unit and the secondary processing unit for comparing a primary output of the primary processing unit and a secondary output of the secondary processing units after the control algorithm has been run by the primary and secondary processing units; and,

at least one bus, wherein the common memory, primary memory and secondary processing units, and function compare module are coupled to the at least one bus, wherein the functional compare module is adapted to read signals on the at least one bus, generate a signature of the signals, compare the generated signature with a reference signal and detect a fault if the signals are not the same.

21. (Original). An apparatus, as set forth in claim 20, wherein the first system is a brake system.

22. (Original). An apparatus, as set forth in claim 20, wherein the first system is a steering system.

23. (Original). An apparatus, as set forth in claim 22, wherein the steering system is a steer by wire system.

24. (Original). An apparatus, as set forth in claim 20, wherein the first system is an engine control system.

25. (Original). An apparatus, as set forth in claim 20, wherein the functional compare module is adapted to detect a fault if the primary output and the secondary output are not the same.

26. (Original). An apparatus, as set forth in claim 20, wherein the primary output and the secondary output are data.

27. (Original). An apparatus, as set forth in claim 20, wherein the primary output and the secondary output are control signals.

28. (Original). An apparatus, as set forth in claim 20, wherein the functional compare module is adapted to perform diagnostics upon startup of the apparatus.

29. (Cancelled).

30. (Currently Amended). An apparatus for controlling a first system of a motor vehicle, ~~as set forth in claim 20, including~~ comprising:

a primary processing unit for performing a first set of functions with respect to the first system;

a secondary processing unit coupled to the primary processing unit;

a common memory coupled to the primary and secondary processing units, the common memory containing a control algorithm, wherein the primary and secondary processing units are adapted to run the control algorithm;

a functional compare module coupled to the primary processing unit and the secondary processing unit for comparing a primary output of the primary processing unit and a secondary output of the secondary processing units after the control algorithm has been run by the primary and secondary processing units; and,

at least one bus, wherein the common memory, primary and secondary processing units, and functional compare module are coupled to the at least one bus, wherein the functional compare module is adapted to read signals on the at least one bus, generate a signature of the signals, compare the generated signature with a reference signal and detect a fault if the signals are not the same.

31. (Original). An apparatus, as set forth in claim 30, wherein the at least one bus includes an address bus, a data bus, and a control bus.

32. (Original). An apparatus, as set forth in claim 20, wherein the secondary processing unit is adapted to control the first system if a fault is detected in the primary processing unit.

33. (Original). An apparatus, as set forth in claim 32, wherein the secondary processing unit is coupled to a second system for control of the second system.

34. (Currently Amended). A method for detecting a fault in a controller for use in a motor vehicle, the controller including a primary processing unit, a secondary processing unit coupled to the primary processing unit, at least one peripheral module coupled to the primary processing unit, and a common memory coupled to the secondary and primary processing units, including the steps of:

reading a control algorithm stored in the common memory by the primary processing unit;

reading the control algorithm stored in the common memory source by the secondary processing unit;

comparing a primary output of the primary processing unit and a secondary output of the secondary processing unit and responsively detecting a fault; and,

detecting faults within the peripheral module using a built in self test circuit coupled to the primary processing unit.

35. (Previously Presented). A method, as set forth in claim 34, wherein the primary processing unit controls a brake system.

36. (Previously Presented). A method, as set forth in claim 34, wherein the primary processing unit controls a steering system.

37. (Previously Presented). A method, as set forth in claim 36, wherein the steering system is a steer by wire system.

38. (Previously Presented). A method, as set forth in claim 34, wherein the primary processing unit controls an engine control system.

39. (Previously Presented). A method, as set forth in claim 34, wherein the primary output and the secondary output are data.

40. (Previously Presented). A method, as set forth in claim 34, wherein the primary output and the secondary output are control signals.

41. (Previously Presented). A method, as set forth in claim 34, including the step of performing diagnostics upon startup of the controller.

42. -58. (Cancelled).